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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,544	01/25/2002	Scott W. Mitchell	TI-32531	3761

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EXAMINER	
TANG, MINH NHUT	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,544	MITCHELL ET AL.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment on 08 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on December 08, 2003. These drawings are approved.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. ***The form and legal phraseology often used in patent claims, such as "means", "comprising" and "said," should be avoided***. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

It is noted that Applicants submitted the amended abstract on December 08, 2003; however, this amended abstract is exactly the same as the original abstract filed on January 25, 2002.

Duplicate Claims

3. Applicant is advised that should claims 23, 25, and 27 be found allowable, claims 24, 26, and 28 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is

proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2, 11-13, and 23-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, the limitation "the solder ball diameter" (lines 2-3) has not been recited previously; therefore this term is indefinite.

In claim 11, the limitation "extending a multiplicity of first conductive probes through said multiplicity of apertures" (lines 10-11, counted by hand) is vague because it is unclear whether or not each conductive probe of the multiplicity of first conductive probes would extend through each corresponding aperture of the multiplicity of apertures. Additionally, it is not clear "a first end" and "a contact end" (line 11) referred to a first and contact ends of which device. For examination purposes, the limitations "extending a multiplicity of first conductive probes through said multiplicity of apertures such that a first end is at said back side and a contact end extends a selected distance beyond said working surface" is interpreted as -- extending each of first conductive probe of a multiplicity of first conductive probes through each aperture of said multiplicity of apertures such that a first end of each first conductive probes is at said

back side and a contact end of each first conductive probes extends a selected distance beyond said working surface.

In claims 23-28, the limitation "the solder ball diameter" (all in line 2) has not been recited previously; therefore this term is indefinite.

Claims 12-13 are rejected since they depend on rejected base claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, and 3-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Noda (U.S.P. 6,404,213).

As to claim 1, Noda discloses, in Fig. 20 (see also Figs. 17 and 18 for similar structure of connecting part), apparatus (31) for simultaneously making electrical contact with an array of contact points (5) having a first selected pattern (i.e., constructed by contact points 5) on a circuit (semiconductor device), comprising: a support substrate (34) having a working surface (i.e., upper surface of substrate 34) and a back side (i.e., lower surface of substrate 34), said support substrate (34) defining a multiplicity of apertures (i.e., holes for inserting probes 21a) extending from said backside (lower surface) through said substrate (34) and terminating at said working

surface (upper surface) according to a second selected pattern corresponding to a mirror image of said first selected pattern; a multiplicity of conductive probes (21a), said conductive probes (21a) extending from a first end (i.e., lower end of probe 21a) at said back side (lower surface) of said support substrate (34), through said apertures (i.e., holes) to a contact end (i.e., upper end of probe 21a corresponding to a portion to which a first land 37 and a second land 38 (Fig. 18) being contacted) located a selected distance beyond said working surface (upper surface) wherein said contact ends (upper ends) of said conductive probes (21a) are substantially flat (see Fig. 18); at least one aperture (i.e., holes for inserting probes 21a) of said multiplicity of apertures including at least two conductive probes (22a, 23a) extending there-through; a multiplicity of conductive pathways (i.e., body of each conductive probes 22a, 23a) extending from said first end (lower end) of said conductive probes (22a, 23a) to selected circuitry; and said conductive probes (22a, 23a) positioned through said support substrate (34) to make electrical contact with contact points (5) on a circuit (semiconductor device) placed against said apparatus (31).

As to claim 3, Noda discloses said contact points (5) are conductive bumps (i.e., pads).

As to claim 4, Noda discloses in column 10, lines 30-35, and column 7, line 41 through column 8, line 15, said at least two conductive probes (22a, 23a) extending through said at least one aperture (i.e., hole) are connected one each to a voltage source line and a voltage sensing device.

As to claim 5, Noda discloses in Fig. 17, a third conductive probe (i.e., another probe(s) 21a adjacent the previous probe) connected to another voltage source.

As to claims 6 and 10, Noda discloses in column 10, line 30, said apparatus (31) is a probe card for testing integrated circuits.

As to claim 7, Noda discloses, in Fig. 20 (see also Figs. 17 and 18 for similar structure of connecting part), an apparatus (31) for simultaneously making electrical contact with an array of contact points (5) positioned according to a first selected pattern (i.e., constructed by contact points 5) on a circuit (semiconductor device) comprising: an insulating support substrate (34) having a working surface (i.e., upper surface of substrate 34) and a back side (i.e., lower surface of substrate 34); a multiplicity of conductive probes (21a), each of said conductive probes (21a) extending from a first end (i.e., lower end of probe 21a) at said backside (lower surface) of said substrate (34), through said substrate (34) to a contact end (i.e., upper end of probe 21a corresponding to a portion to which a first land 37 and a second land 38 (Fig. 18) being contacted), contact ends (upper ends) of said multiplicity of conductive probes (21a) extending a selected distance beyond said working surface (upper surface) and terminating at a multiplicity of locations (i.e., locations for making connection with wiring 36 in Fig. 17) arranged according to a second selected pattern corresponding to a mirror image of said first selected pattern and wherein said contact ends (upper ends) of said conductive probes (21a) are substantially flat (see Fig. 18); at least two conductive probes (22a, 23a) of said multiplicity of conductive probes (21a) having their ends adjacent each other at a single one of said multiplicity of locations (see Fig. 20); and

said contact ends (upper ends) of said conductive probes (22a, 23a) positioned through said support substrate (34) to make electrical contact with selected ones of said contact points (5) on a circuit placed against said apparatus (31).

As to claim 8, Noda discloses in Figs. 17 and 20, at least two of said multiplicity of locations include at least two of said conductive probes (21a).

As to claim 9, Noda discloses in Figs. 17 and 20, at least two of said multiplicity of locations include at least three of said conductive probes (21a).

As to claim 11, Noda discloses, in Fig. 20 (see also Figs. 17 and 18 for similar structure of connecting part), a method of manufacturing apparatus (31) for simultaneously making electrical contact with an array of contact points (5) on circuitry (semiconductor device), said array of contact points (5) positioned according to a first selected pattern (i.e., constructed by contact points 5), comprising the steps of: providing a support substrate (34) having a working surface (i.e., upper surface of substrate 34) and a backside (i.e., lower surface of substrate 34); defining a multiplicity of apertures (i.e., holes for inserting probes 21a) extending from said backside (lower surface) through said substrate (34) and terminating at said working surface (upper surface) according to a second selected pattern, said second selected pattern corresponding to a mirror image of said first selected pattern; extending each of first conductive probe (22a) of a multiplicity of first conductive probes (also called 22a) through each aperture (hole) of said multiplicity of apertures (holes) such that a first end (i.e., lower end of probe 22a) of each first conductive probes (22a) is at said back side (lower surface) and a contact end (i.e., upper end of probe 22a corresponding to a

portion to which a first land 37 (Fig. 18) being contacted) of each first conductive probes (22a) extends a selected distance beyond said working surface (upper surface); extending a second conductive probe (23a) having a first end (i.e., lower end of probe 23a) and a contact end (i.e., upper end of probe 23a corresponding to a portion to which a second land 38 (Fig. 18) being contacted) through at least one of said multiplicity of apertures (holes); and positioning said multiplicity of apertures (holes) such that said contact ends (upper ends) of said first conductive probes (22a) and said second conductive probe (23a) are aligned to make electrical contact with at least a portion of said array of contact points (5) of a circuit (semiconductor device) placed against said apparatus (31) and wherein said contact end (upper end) of said first conductive probes (22a) and said second conductive probes (23a) are substantially flat (see Fig. 18).

As to claims 12 and 15, Noda discloses in Figs. 17 and 20, placing circuitry (semiconductor device) having an array of contact points (5) against said apparatus (31) and testing said circuitry (semiconductor device).

As to claims 13 and 16, Noda discloses in column 10, lines 30-35, and column 7, line 41 through column 8, line 15, a selected probe (22a) of said multiplicity of first conductive probes (22a) is for supplying a selected voltage and said second conductive probe (23a) adjacent said selected probe (22a) is for sensing a voltage.

As to claim 14, Noda discloses, in Fig. 20 (see also Figs. 17 and 18 for similar structure of connecting part), a method of manufacturing apparatus (31) for simultaneously making electrical contact with an array of contact points (5) on circuits (semiconductor devices), said array of contact points (5) positioned according to a first

selected pattern (i.e., constructed by contact points 5), comprising the steps of: providing a support substrate (34) having a backside (i.e., lower surface of substrate 34) and a working surface (i.e., upper surface of substrate 34); extending a multiplicity of first conductive probes (22a) through said support substrate (34), each of said first conductive probes (22a) extending from a first end (i.e., lower end of probe 22a) at said backside (lower surface) of said substrate (34), through said substrate (34) to a contact end (i.e., upper end of probe 22a corresponding to a portion to which a first land 37 (Fig. 18) being contacted), said contact ends (upper ends) of said conductive probes (22a) extending a selected distance beyond said working surface (upper surface) and terminating at a multiplicity of locations (i.e., locations for making connection with wiring 36 in Fig. 17) according to a second selected pattern corresponding to a mirror image of said first selected pattern; extending at least one second conductive probe (23a) having a first end (i.e., lower end of probe 23a) and a contact end (i.e., upper end of probe 23a corresponding to a portion to which a second land 38 (Fig. 18) being contacted) through said substrate (34), said contact end (upper end) of said at least one second conductive probe (23a) terminating adjacent the contact end (upper end) of one of said multiplicity of first conductive probes (22a); and positioning said first conductive probes (22a) and said second conductive probe (23a) such that said contact ends (upper ends) of said first conductive probes (22a) and said second conductive probe (23a) are aligned so as to make electrical contact with said array of contact points (5) of a circuit (semiconductor device) placed against said apparatus (31) and wherein said contact

ends (upper ends) of said first and second conductive probes (22a, 23a) are substantially flat (see Fig. 18).

Response to Arguments

8. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Applicants, on page 9 or the Remarks, asserted that the contact needles of the present invention have a flat tip that is not shown in the Noda reference. The Examiner respectfully disagrees because, as shown in Figs. 18 and 20 of the Noda reference, the probe has both distal end and proximal end be substantially flat.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mrs. Cuneo, Kamand can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Minh Tang

02/27/04